IN THE CLAIMS

Please cancel Claim 29 without prejudice or disclaimer.

Claim 1 (original): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter.

Claim 2 (previously presented): A digital filter circuit according to claim 1, wherein said digital filter circuit is configured such that said first digital filter is selected to receive and filter samples of data during a first delay cycle and provide a filtered data output signal corresponding to said samples received during the first delay cycle and said second digital filter is selected to receive and filter a first sample of data during the first delay cycle and a delayed sample of data during a delay cycle subsequent to the first delay cycle and to provide a filtered data output signal corresponding to said samples received during the first delay cycle and the subsequent delay cycle.

Claim 3 (original): A digital filter according to claim 1, wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution.

Claim 4 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein said first digital filter comprises at least a one-delay filter, said second digital filter comprises a two-delay filter, and said third digital filter comprises a three or greater-delay filter.

Claim 5 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a

composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein said first digital filter comprises a sinc1 filter, said second digital filter comprises a sinc2 filter, and said third digital filter comprises a sinc3 filter.

Claim 6 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein said first digital filter and said second digital filter comprise a sinc2 filter, and said third digital filter comprises a sinc3 filter.

Claim 7 (original): A digital filter according to claim 6, wherein said first digital filter is coupled with a notch filter configured to replace a first, third and a subsequent odd-order harmonic notch of said first digital filter.

Claim 8 (original): A digital filter according to claim 6, wherein said first filter is configured with a decimation ratio lower than a decimation ratio of said second filter.

Claim 9 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein said digital filter circuit comprises a switching mechanism for selecting one of said first digital filter, said second digital filter and said third digital filter to receive, filter and output sampled data.

Claim 10 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein each said first digital filter, said second digital filter, and said third digital filter comprise a separate filter path, and wherein a gain parameter of each said separate filter path is matched to a gain parameter of any other said separate filter path to provide an equalized gain.

Claim 11 (original): A digital filter according to claim 9, wherein said gain parameters are matched as a function of a decimation ratio of one of said first digital filter, said second digital filter, and said third digital filter.

Claim 12 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter arrangement configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution, and

wherein the parallel arrangement is configured to provide reduced layout requirements, said third digital filter comprising three integrators in series with three differentiators, said second digital filter shares at least two of said three integrators, and said first digital filter shares at least one of said three integrators.

Claim 13 (original): An analog-to-digital converter having a fast settling time, said analog-to-digital filter comprising:

a multiplexor having a plurality of input channels;

a modulator for receiving an output from one of said plurality of input channels of said multiplexor; and

a digital filter circuit for receiving an output from said modulator and for providing a filtered output, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate, and a second level of noise resolution that is higher than said first level of

noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter configured to facilitate a faster settling and response time for said digital filter.

Claim 14 (original): An analog-to-digital converter according to claim 13, wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution.

Claim 15 (original): An analog-to-digital converter according to claim 14, wherein said digital filter circuit is configured such that said first digital filter is selected to receive and filter samples of data during a first delay cycle to provide a first output signal corresponding to said samples received during the first delay cycle, said second digital filter is selected to receive and filter samples of data during the first delay cycle and a second delay cycle to provide a second output signal corresponding to said samples received during the first delay cycle and the second delay cycle, and said third digital filter is selected to receive and filter samples of data during a delay cycle subsequent to the second delay cycle to provide a third output signal corresponding to said samples received during the first delay cycle, the second delay cycle and the subsequent delay cycle.

Claim 16 (previously presented): An analog-to-digital converter having a fast settling time, said analog-to-digital filter comprising:

a multiplexor having a plurality of input channels;

a modulator for receiving an output from one of said plurality of input channels of said multiplexor; and

a digital filter circuit for receiving an output from said modulator and for providing a filtered output, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate, and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution,

wherein the parallel arrangement is configured to provide reduced layout requirements, said third digital filter comprising three integrators in series with three differentiators, said second digital filter shares at least two of said three integrators, and said first digital filter shares at least one of said three integrators.

Claim 17 (previously presented): An analog-to-digital converter having a fast settling time, said analog-to-digital filter comprising:

a multiplexor having a plurality of input channels;

a modulator for receiving an output from one of said plurality of input channels of said multiplexor; and

a digital filter circuit for receiving an output from said modulator and for providing a filtered output, said digital filter circuit comprising:

a first digital filter having a first settling rate and a first level of noise resolution; and

a second digital filter configured in a parallel arrangement with said first digital filter, said second digital filter having a second settling rate that is slower than said first settling rate, and a second level of noise resolution that is higher than said first level of noise resolution, wherein said first digital filter and said second digital filter comprise a composite filter configured to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter configured in a parallel arrangement with said first digital filter and said second digital filter, said third digital filter having a third settling rate that is slower than said second settling rate, and a third level of noise resolution that is higher than said second level of noise resolution,

wherein said third digital filter comprises an order of delay configuration one order higher than an order configuration of said modulator.

Claim 18 (original): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter selected to receive and filter samples of data during an initial delay cycle and provide a first output data signal corresponding to the samples received during the initial delay cycle; and

a second digital filter having a settling rate that is slower than a settling rate of said first digital filter, and a level of noise resolution that is higher than a level of noise resolution of said first digital filter, said second digital filter being selected to receive and filter samples of data during a subsequent delay cycle and to provide a second output data signal corresponding to samples received during the subsequent delay cycle, and

wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter.

Claim 19 (original): A digital filter according to claim 18, wherein said digital filter circuit further comprises a third digital filter having a settling rate that is slower than said settling rate of said second digital filter, and a level of noise resolution that is higher than said level of noise resolution of said second digital filter.

Claim 20 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter selected to receive and filter samples of data during an initial delay cycle and provide a first output data signal corresponding to the samples received during the initial delay cycle; and

a second digital filter having a settling rate that is slower than a settling rate of said first digital filter, and a level of noise resolution that is higher than a level of noise resolution of said first digital filter, said second digital filter being selected to receive and filter samples of data during a subsequent delay cycle and to provide a second output data signal corresponding to samples received during the subsequent delay cycle, and

wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter having a settling rate that is slower than said settling rate of said second digital filter, and a level of noise resolution that is higher than said level of noise resolution of said second digital filter, and

wherein said first digital filter comprises at least a one-delay filter, said second digital filter comprises a two-delay filter, and said third digital filter comprises at least a three-delay filter.

Claim 21 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter selected to receive and filter samples of data during an initial delay cycle and provide a first output data signal corresponding to the samples received during the initial delay cycle; and

a second digital filter having a settling rate that is slower than a settling rate of said first digital filter, and a level of noise resolution that is higher than a level of noise resolution of said first digital filter, said second digital filter being selected to receive and filter samples of data during a subsequent delay cycle and to provide a second output data signal corresponding to samples received during the subsequent delay cycle, and

wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter having a settling rate that is slower than said settling rate of said second digital filter, and a level of noise resolution that is higher than said level of noise resolution of said second digital filter, and

wherein each of said first digital filter and said second digital filter comprise a sinc2 filter, and said third digital filter comprises a sinc3 filter.

Claim 22 (previously presented): A digital filter circuit for use in an analog-to-digital converter, said digital filter circuit comprising:

a first digital filter selected to receive and filter samples of data during an initial delay cycle and provide a first output data signal corresponding to the samples received during the initial delay cycle; and

a second digital filter having a settling rate that is slower than a settling rate of said first digital filter, and a level of noise resolution that is higher than a level of noise

resolution of said first digital filter, said second digital filter being selected to receive and filter samples of data during a subsequent delay cycle and to provide a second output data signal corresponding to samples received during the subsequent delay cycle, and

wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter,

wherein said digital filter circuit further comprises a third digital filter having a settling rate that is slower than said settling rate of said second digital filter, and a level of noise resolution that is higher than said level of noise resolution of said second digital filter, and

wherein said first digital filter is coupled with a notch filter configured to replace a first, third and a subsequent odd-order harmonic notch of said first digital filter.

Claim 23 (original): A digital filter according to claim 19, wherein said first digital filter is configured with a lower decimation rate than said second digital filter and said third digital filter.

Claim 24 (previously presented): A digital filter according to claim 19, wherein each said first digital filter comprises a first filter path having a first gain component, said second digital filter comprises a second filter path having a second gain component, and said third digital filter comprises a third filter path having a third gain component, and wherein said digital filter circuit includes at least two multipliers configured within said two of said filter paths, said multipliers configured to provide equalized gains within each said filter paths.

Claim 25 (previously presented): A method of providing for the faster settling of data by a digital filter after the switching of input channels in a multiplexor used in an analog-to-digital converter, said method comprising the steps of:

selecting a first digital filter to receive samples of data from an output of a modulator during a first delay cycle, said first digital filter having a first settling rate and a first level of noise resolution;

providing a filtered data output signal corresponding to said samples received during the first data cycle;

selecting a second digital filter to receive samples of data from the output of the modulator during the first delay cycle and a subsequent delay cycle, said second digital filter configured in a parallel arrangement with said first digital filter and having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the first delay cycle and the subsequent data cycle, wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter.

Claim 26 (original): A method according to claim 25, wherein said second digital filter receives samples of data from the output of the modulator during a second delay cycle and provides a filtered data output signal corresponding to said samples received during the second delay cycle, and wherein said method further comprises the steps of:

selecting a third digital filter to receive samples of data from the output of the modulator during a delay cycle subsequent to the second delay cycle, said third digital filter configured in a parallel arrangement with said second digital filter and having a third settling rate that is slower than said second settling rate and a third level of noise resolution that is higher than said second level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the delay cycle subsequent to the second delay cycle.

Claim 27 (previously presented): A method of providing for the faster settling of data by a digital filter after the switching of input channels in a multiplexor used in an analog-to-digital converter, said method comprising the steps of:

selecting a first digital filter to receive samples of data from an output of a modulator during a first delay cycle, said first digital filter having a first settling rate and a first level of noise resolution;

providing a filtered data output signal corresponding to said samples received during the first data cycle;

selecting a second digital filter to receive samples of data from the output of the modulator during the first delay cycle and a subsequent delay cycle, said second digital filter configured in a parallel arrangement with said first digital filter and having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the first delay cycle and the subsequent data cycle, wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter,

wherein said second digital filter receives samples of data from the output of the modulator during a second delay cycle and provides a filtered data output signal corresponding to said samples received during the second delay cycle, and wherein said method further comprises the steps of:

selecting a third digital filter to receive samples of data from the output of the modulator during a delay cycle subsequent to the second delay cycle, said third digital filter configured in a parallel arrangement with said second digital filter and having a third settling rate that is slower than said second settling rate and a third level of noise resolution that is higher than said second level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the delay cycle subsequent to the second delay cycle,

wherein said method further comprises the step of matching a gain parameter of a filter path for each of said first filter, said second filter and said third filter to provide an equalized gain.

Claim 28 (previously presented): A method of providing for the faster settling of data by a digital filter after the switching of input channels in a multiplexor used in an analog-to-digital converter, said method comprising the steps of:

selecting a first digital filter to receive samples of data from an output of a modulator during a first delay cycle, said first digital filter having a first settling rate and a first level of noise resolution;

providing a filtered data output signal corresponding to said samples received during the first data cycle;

selecting a second digital filter to receive samples of data from the output of the modulator during the first delay cycle and a subsequent delay cycle, said second digital filter configured in a parallel arrangement with said first digital filter and having a second settling rate that is slower than said first settling rate and a second level of noise resolution that is higher than said first level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the first delay cycle and the subsequent data cycle, wherein said first digital filter and said second digital filter are configured in a composite arrangement to facilitate a faster settling and response time for said digital filter,

wherein said second digital filter receives samples of data from the output of the modulator during a second delay cycle and provides a filtered data output signal corresponding to said samples received during the second delay cycle, and wherein said method further comprises the steps of:

selecting a third digital filter to receive samples of data from the output of the modulator during a delay cycle subsequent to the second delay cycle, said third digital filter configured in a parallel arrangement with said second digital filter and having a

third settling rate that is slower than said second settling rate and a third level of noise resolution that is higher than said second level of noise resolution; and

providing a filtered data output signal corresponding to said samples received during the delay cycle subsequent to the second delay cycle,

wherein said first filter is configured with a notch filter for replacing a first, third any a subsequent odd-order harmonic notch of said first filter circuit.

Claim 29 (cancelled).